APPLICATION NOTE

AN170
NE555 and NE556 applications

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INTRODUCTION

In mid 1972, Philips Semiconductors introduced the 555 timer, a unique functional building block that has enjoyed unprecedented popularity. The timer's success can be attributed to several inherent characteristics foremost of which are versatility, stability and low cost. There can be no doubt that the 555 timer has altered the course of the electronics industry with an impact not unlike that of the IC operational amplifier.

The simplicity of the timer, in conjunction with its ability to produce long time delays in a variety of applications, has lured many designers from mechanical timers, op amps, and various discrete circuits into the ever increasing ranks of timer users.

DESCRIPTION

The 555 timer consists of two voltage comparators, a bistable flip-flop, a discharge transistor, and a resistor divider network. To understand the basic concept of the timer let's first examine the timer in block form as in Figure 1.

The resistive divider network is used to set the comparator levels. Since all three resistors are of equal value, the threshold comparator is referenced internally at 2/3 of supply voltage level and the trigger comparator is referenced at 1/3 of supply voltage. The outputs of the comparators are tied to the bistable flip-flop. When the trigger voltage is moved below 1/3 of the supply, the comparator changes state and sets the flip-flop driving the output to a high state. The threshold pin normally monitors the capacitor voltage of the RC timing network. When the

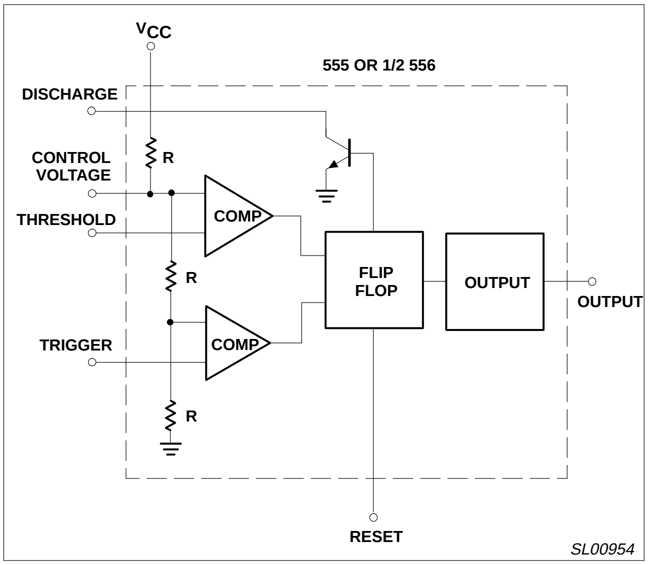


Figure 1. 555/556 Timer Functional Block Diagram

capacitor voltage exceeds 2/3 of the supply, the threshold comparator resets the flip-flop which in turn drives the output to a low state. When the output is in a low state, the discharge transistor is "on", thereby discharging the external timing capacitor. Once the capacitor is discharged, the timer will await another trigger pulse, the timing cycle having been completed.

The 555 and its complement, the 556 Dual Timer, exhibit a typical initial timing accuracy of 1% with a 50ppm/C timing drift with temperature. To operate the timer as a one-shot, only two external components are necessary; resistance & capacitance. For an oscillator, only one additional resistor is necessary. By proper selection of external components, oscillating frequencies from one cycle per half hour to 500kHz can be realized. Duty cycles can be adjusted from less than one percent to 99 percent over the frequency spectrum. Voltage control of timing and oscillation functions is also available.

Timer Circuitry

The timer is comprised of five distinct circuits: two voltage comparators; a resistive voltage divider reference; a bistable flip-flop; a discharge transistor; and an output stage that is the "totem-pole" design for sink or source capability. Q_{10}-Q_{13} comprise a Darlington differential pair which serves as a trigger comparator. Starting with a positive voltage on the trigger, Q_{10} and Q_{11} turn on when the voltage at Pin 2 is moved below one third of the supply voltage. The voltage level is derived from a resistive divider chain consisting of R_7, R_8 and R_9. All three resistors are of equal value (5kΩ). At 15V supply, the triggering level would be 5V.
When Q_{10} and Q_{11} turn on, they provide a base drive for Q_{15}, turning it on. Q_{16} and Q_{17} form a bistable flip-flop. When Q_{15} is saturated, Q_{16} is "off' and Q_{17} is saturated. Q_{16} and Q_{17} will remain in these states even if the trigger is removed and Q_{15} is turned "off'. While Q_{17} is saturated, Q_{20} and Q_{14} are turned off.

The output structure of the timer is a "totem-pole" design, with Q_{22} and Q_{24} being large geometry transistors capable of providing 200mA with a 15V supply. While Q_{20} is "off', base drive is provided for Q_{22} by Q_{21}, thus providing a high output.

For the duration that the output is in a high state, the discharge transistor is "off'. Since the collector of Q_{14} is typically connected to the external timing capacitor, C, while Q_{14} is off, the timing capacitor now can charge through the timing resistor, R_A.

The capacitor voltage is monitored by the threshold comparator (Q_1-Q_4) which is a Darlington differential pair. When the capacitor voltage reaches two thirds of the supply voltage, the current is directed from Q_3 and Q_4 thru Q_1 and Q_2. Amplification of the current change is provided by Q_5 and Q_6. Q_5-Q_6 and Q_7-Q_8 comprise a diode-biased amplifier. The amplified current change from Q_6 now provides a base drive for Q_{16} which is part of the bistable flip-flop, to change states. In doing so, the output is driven "low", and Q_{14}, the discharge transistor, is turned "on", shorting the timing capacitor to ground.

The discussion to this point has only encompassed the most fundamental of the timer's operating modes and circuitry. Several points of the circuit are brought out to the real world which allow the timer to function in a variety of modes. It is essential that one understands all the variations possible in order to utilize this device to its fullest extent.

Reset Function

Regressing to the trigger mode, it should be noted that once the device has triggered and the bistable flip-flop is set, continued triggering will not interfere with the timing cycle. However, there may come a time when it is necessary to interrupt or halt a timing cycle. This is the function that the reset accomplishes.

In the normal operating mode the reset transistor, Q_{25}, is off with its base held high. When the base of Q_{25} is grounded, it turns on, providing base drive to Q_{14}, turning it on. This discharges the timing capacitor, resets the flip-flop at Q_{17}, and drives the output low. The reset overrides all other functions within the timer.

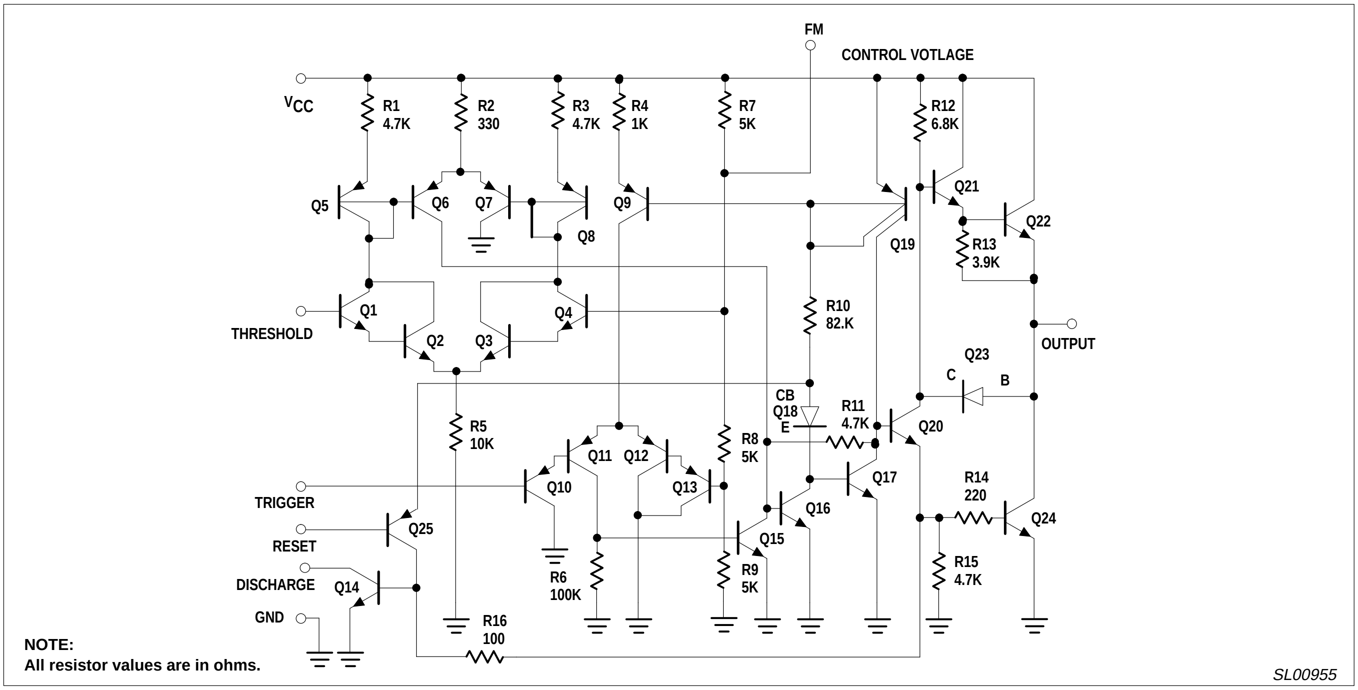


Figure 2. Schematic of 555 or 1/2 556 Dual Timer

Trigger Requirements

Due to the nature of the trigger circuitry, the timer will trigger on the negative-going edge of the input pulse. For the device to time-out properly, it is necessary that the trigger voltage level be returned to some voltage greater than one third of the supply before the timeout period. This can be achieved by making either the trigger pulse sufficiently short or by AC coupling into the trigger. By AC coupling the trigger (see Figure 3), a short negative-going pulse is achieved when the trigger signal goes to ground. AC coupling is most frequently used in conjunction with a switch or a signal that goes to ground which initiates the timing cycle. Should the trigger be held low, without AC coupling, for a longer duration than the timing cycle the output will remain in a high state for the duration of the low trigger signal, without regard to the threshold comparator state. This is due to the predominance of Q_{15} on the base of Q_{16}, controlling the state of the bistable flip-flop. When the trigger signal then returns to a high level, the output will fall immediately. Thus, the output signal will follow the trigger signal in this case.

Control Voltage

One additional point of significance, the control voltage, is brought out on the timer. As mentioned earlier, both the trigger comparator, Q_{10}-Q_{13}, and the threshold comparator, Q_1-Q_4, are referenced to an internal resistor divider network, R_7, R_8, R_9. This network establishes the nominal two thirds of supply voltage (V_{CC}) trip point for the threshold comparator and one third of V_{CC} for the trigger comparator. The two thirds point at the junction of R_7, R_8 and the base of Q_4 is brought out. By imposing a voltage at this point, the comparator reference levels may be shifted either higher or lower than the nominal levels of one third and two thirds of the supply voltage. Varying the voltage at this point will vary the timing. This feature of the timer opens a multitude of application possibilities such as using the timer as a voltage-controlled oscillator, pulse-width modulator, etc. For applications where the control voltage function is not used, it is strongly recommended that a bypass capacitor (0.01µF) be placed across the control voltage pin and ground. This will increase the noise immunity of the timer to high frequency trash which may monitor the threshold levels causing timing error.

Monostable Operation

The timer lends itself to three basic operating modes:

1. Monostable (one-shot)
2. Astable (oscillatory)
3. Time delay

By utilizing one or any combination of basic operating modes and suitable variations, it is possible to utilize the timer in a myriad of applications. The applications are limited only to the imagination of the designer.

One of the simplest and most widely used operating modes of the timer is the monostable (one-shot). This configuration requires only two external components for operation (see Figure 4). The sequence of events starts when a voltage below one third V_{CC} is sensed by the trigger comparator. The trigger is normally applied in the form of a short negative-going pulse. On the negative-going edge of the pulse, the device triggers, the output goes high and the discharge transistor turns off. Note that prior to the input pulse, the discharge transistor is on, shorting the timing capacitor to ground. At this point the timing capacitor, C, starts charging through the timing resistor, R. The voltage on the capacitor increases exponentially with a time constant T=RC. Ignoring capacitor leakage, the capacitor will reach the two thirds V_{CC} level in 1.1 time constants or

$$T = 1.1\ RC \qquad (1)$$

Where T is in seconds, R is in ohms, and C is in Farads. This voltage level trips the threshold comparator, which in turn drives the output low and turns on the discharge transistor. The transistor discharges the capacitor, C, rapidly. The timer has completed its cycle and will now await another trigger pulse.

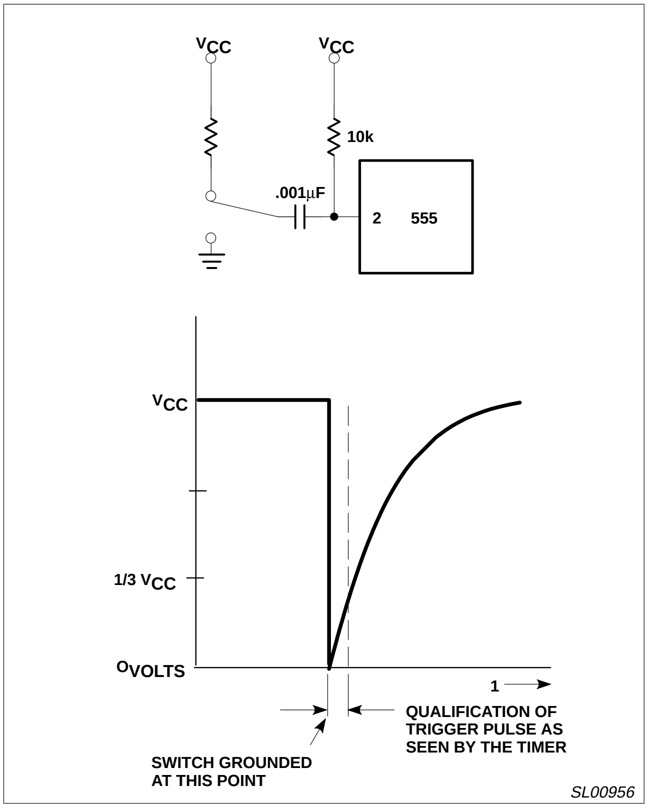


Figure 3. AC Coupling of the Trigger Pulse

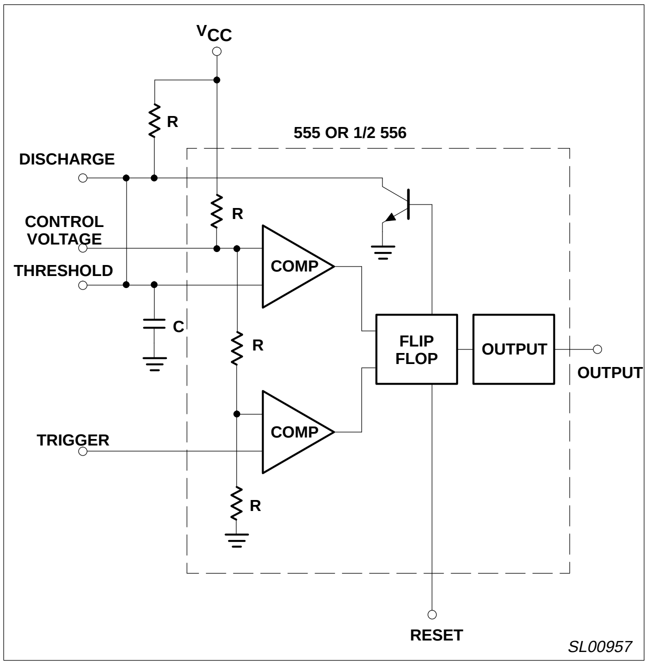


Figure 4. Monostable Operation

Astable Operation

In the astable (free-run) mode, only one additional component, R_B, is necessary. The trigger is now tied to the threshold pin. At power-up, the capacitor is discharged, holding the trigger low. This triggers the timer, which establishes the capacitor charge path through R_A and R_B. When the capacitor reaches the threshold level of 2/3 V_{CC}, the output drops low and the discharge transistor turns on.

The timing capacitor now discharges through R_B. When the capacitor voltage drops to 1/3 V_{CC}, the trigger comparator trips, automatically retriggering the timer, creating an oscillator whose frequency is given by:

$$f = \frac{1.49}{(R_A + 2R_B)\ C} \qquad (2)$$

Selecting the ratios of R_A and R_B varies the duty cycle accordingly. Lo and behold, we have a problem. If a duty cycle of less than fifty percent is required, then what? Even if R_A=0, the charge time cannot be made smaller than the discharge time because the charge path is R_A+R_B while the discharge path is R_B alone. In this case it becomes necessary to insert a diode in parallel with R_B, cathode toward the timing capacitor. Another diode is desirable, but not mandatory (this one in series with R_B), cathode away from the timing capacitor. Now the charge path becomes R_A, through the parallel diode into C. Discharge is through the series diode and R_B to the discharge transistor. This scheme will afford a duty cycle range from less than 5% to greater than 95%. It should be noted that for reliable operation a minimum value of 3kΩ for R_B is recommended to assure that oscillation begins.

Time Delay

In this third basic operating mode, we aim to accomplish something a little different from monostable operation. In the monostable mode, when a trigger was applied, immediately changed to the high state, timed out, and returned to its pre-trigger low state. In the time delay mode, we require the output not to change state upon triggering, but at some precalculated time after trigger is received.

The threshold and trigger are tied together, monitoring the capacitor voltage. The

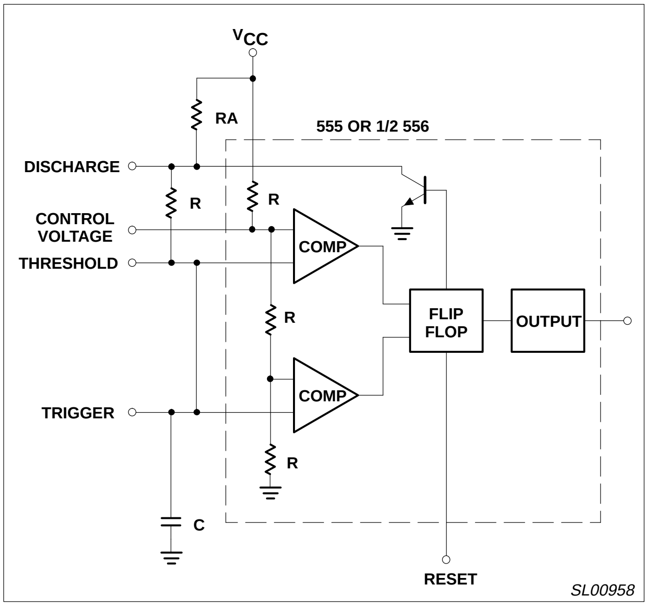


Figure 5. Astable Operation

discharge function is not used. The operation sequence begins as transistor (T_1) is turned on, keeping the capacitor grounded. The trigger sees a low state and forces the timer output high. When the transistor is turned off, the capacitor commences its charge cycle. When the capacitor reaches the threshold level, only then does the output change from its normally high state to the low state. The output will remain low until T_1 is again turned on.

GENERAL DESIGN CONSIDERATIONS

The timer will operate over a guaranteed voltage range of 4.5V to $15V_{DC}$ with $16V_{DC}$ being the absolute maximum rating. Most of the devices, however, will operate at voltage levels as low as $3V_{DC}$. The timing interval is independent of supply voltage since the charge rate and threshold level of the comparator are both directly proportional to supply. The supply voltage may be provided by any number of sources, however, several precautions should be taken. The most important, the one which provides the most headaches if not practiced, is good power supply filtering and adequate bypassing. Ripple on the supply line can cause loss of timing accuracy. The threshold level shifts, causing a change of charging current. This will cause a timing error for that cycle.

Due to the nature of the output structure, a high power totem-pole design, the output of the timer can exhibit large current spikes on the supply line. Bypassing is necessary to eliminate this phenomenon. A capacitor across the V_{CC} and ground, directly across the device, is necessary and ideal. The size of a capacitor will depend on the specific application. Values of capacitance from 0.01µF to 10µF are not uncommon, but note that the bypass capacitor would be as close to the device as physically possible.

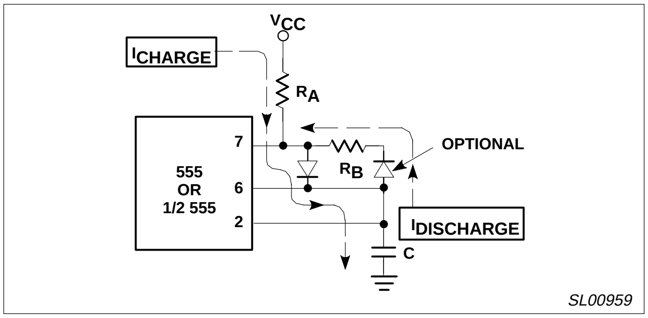


Figure 6. Method of Achieving Duty Cycles Less Than 50%

Selecting External Components

In selecting the timing resistor and capacitor, there are several considerations to be taken into account.

Stable external components are necessary for the RC network if good timing accuracy is to be maintained. The timing resistor(s) should be of the metal film variety if timing accuracy and repeatability are important design criteria. The timer exhibits a typical initial accuracy of one percent. That is, with any one RC network, from timer to timer only one percent change is to be expected. Most of the initial timing error (i.e., deviation from the formula) is due to inaccuracies of external components. Resistors range from their rated values by 0.01% to 10% and 20%. Capacitors may have a 5% to 10% deviation from rated capacity. Therefore, in a system where timing is critical, an adjustable timing resistor or precision components are necessary. For best results, a good quality trim pot, placed in series with the largest feasible resistance, will allow for best adjustability and performance.

The timing capacitor should be a high quality, stable component with very low leakage characteristics. Under no circumstances should ceramic disc capacitors be used in the timing network! Ceramic disc capacitors are not sufficiently stable in capacitance to operate properly in an RC mode. Several acceptable capacitor types are: silver mica, mylar, polycarbonate, polystyrene, tantalum, or similar types.

The timer typically exhibits a small negative temperature coefficient (50ppm/°C). If timer accuracy over temperature is a consideration, timing components with a small positive temperature coefficient should be chosen. This combination will tend to cancel timing drift due to temperature.

In selecting the values for the timing resistors and capacitor, several points should be considered. A minimum value of threshold current is necessary to trip the threshold comparator. This value is 0.25µA. To calculate the maximum value of resistance, keep in mind that at the time the threshold current is required, the voltage potential on the threshold pin is two thirds of supply. Therefore:

$$V_{potential} = V_{CC} - V_{Capacitor}$$

$$V_{potential} = V_{CC} - 2/3V_{CC} = 1/3V_{CC}$$

Maximum resistance is then defined as

$$R_{MAX} = \frac{V_{CC} \quad V_{CAP}}{I_{THRESH}} \qquad (3)$$

Example: $V_{CC} = 15V$

$$R_{MAX} = \frac{15 \quad 10}{0.25(10^{\ 6})} = 20M\Omega$$

$V_{CC} = 5V$

$$R_{MAX} = \frac{5 \quad 3.33}{0.25(10^{\ 6})} = 6.6M\Omega$$

NOTE:
If using a large value of timing resistor, be certain that the capacitor leakage is significantly lower than the charging current available to minimize timing error.

On the other end of the spectrum, there are certain minimum values of resistance that should be observed. The discharge transistor, Q_{14}, is current-limited at 35mA to 55mA internally. Thus, at the current limiting values, Q_{14} establishes high saturation voltages. When examining the currents at Q_{14}, remember that the transistor, when turned on, will be carrying two current loads. The first being the constant current through timing resistor, R_A. The second will be the varying discharge current from the timing capacitor. To provide best operation, the current contributed by the R_A path should be minimized so that the majority of discharge current can be used to reset the capacitor voltage. Hence it is recommended that a 5kΩ value be the minimum feasible value for R_A. This does not mean lower values cannot be used successfully in certain applications, yet there are extreme cases that should be avoided if at all possible.

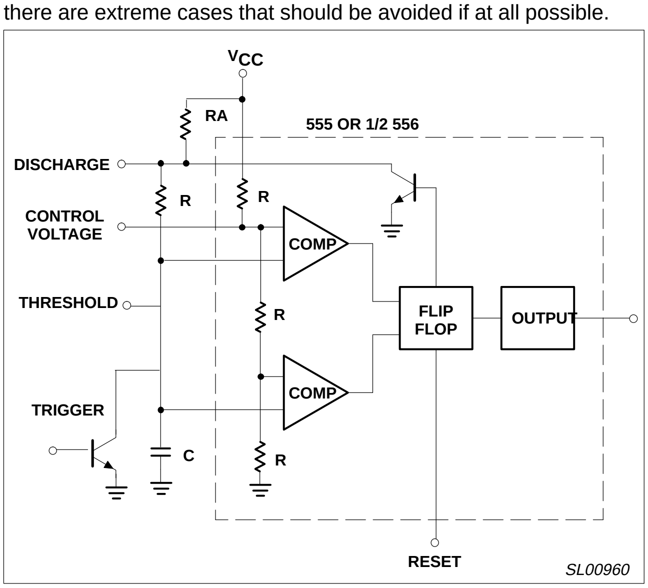


Figure 7. Time Delay Operation

Capacitor size has not proven to be a legitimate design criteria. Values ranging from picofarads to greater than one thousand microfarads have been used successfully. One precaution need be utilized, though. (It should be a cardinal rule that applies to the usage of all ICs.) Make certain that the package power dissipation is not exceeded. With extremely large capacitor values, a maximum duty cycle which allows some cooling time for the discharge transistor may be necessary.

The most important characteristic of the capacitor should be as low a leakage as possible. Obviously, any leakage will subtract from the charge count, causing the calculated time to be longer than anticipated.

Control Voltage

Regressing momentarily, we recall that the control voltage pin is connected directly to the threshold comparator at the junction of R_7, or
R_8. The combination of R_7, R_8 and R_9 comprises the resistive voltage divider network that establishes the nominal V_{CC} trigger comparator level (junction R_8, R_9) and the V_{CC} level for the threshold comparator (junction R_7, R_8).

For most applications, the control voltage function is not used and therefore is bypassed to ground with a small capacitor for noise filtering. The control voltage function, in other applications, becomes an integral part of the design. By imposing a voltage at this pin, it becomes possible to vary the threshold comparator “set” level above or below the 2/3 V_{CC} nominal, thereby varying the timing. In the monostable mode, the control voltage may be varied from 45% to 90% of V_{CC}. The 45-90% figure is not firm, but only an indication to a safe usage. Control voltage levels below and above those stated have been used successfully in some applications.

In the oscillatory (free-run) mode, the control voltage limitations are from 1.7V to V_{CC}. These values should be heeded for reliable operation. Keep in mind that in this mode the trigger level is also important. When the control voltage raises the threshold comparator level, it also raise the trigger comparator level by one-half that amount due to R_8 and R_9 of Figure 2. As a voltage-controlled oscillator, one can expect ±25% around center frequency (f_O) to be virtually linear with a normal RC timing circuit. For wider linear variations around f_O it may be desirable to replace the charging resistor with a constant-current source. In this manner, the exponential charging characteristics of the classical configuration will be altered to linear charge time.

Reset Control

The only remaining function now is the reset. As mentioned earlier, the reset, when taken to ground, inhibits all device functioning. The output is driven low, the bistable flip-flop is reset, and the timing capacitor is discharged. In the astable (oscillatory) mode, the reset can be used to gate the oscillator. In the monostable, it can be used as a timing abort to either interrupt a timing sequence or establish a standby mode (i.e., device off during power-up). It can also be used in conjunction with the trigger pin to establish a positive edge-triggered circuit as opposed to the normal negative edge-trigger mode. One thing to keep in mind when using the reset function is that the reset voltage (switching) point is between 0.4V and 1.0V (min/max). Therefore, if used in conjunction with the trigger, the device will be out of the reset mode prior to reaching 1V. At that point the trigger is in the “turn on” region, below 1/3 V_{CC}. This will cause the device to trigger immediately, effectively triggering on the positive-going edge if a pulse is applied to Pins 4 and 2 simultaneously.

FREQUENTLY ASKED APPLICATIONS QUESTIONS

The following is a harvest of various maladies, exceptions, and idiosyncrasies that may exhibit themselves from time to time in

various applications. Rather than cast aspersions, a quick review of this list may uncover a solution to the problem at hand.

1. In the oscillator mode when reset is released the first time constant is approximately twice as long as the rest. Why?
   Answer: In the oscillator mode the capacitor voltage fluctuates between 1/2 and 2/3 of the supply voltage. When reset is pulled down, the capacitor discharges completely. Thus for the first cycle it must charge from ground to 2/3 V_{CC}, which takes twice as long.
2. What is maximum frequency of oscillations?
   Answer: Most devices will oscillate about 1MHz. However, in the interest of temperature stability, one should operate only up to about 500kHz.
3. What is temperature drift for oscillator mode?
   Answer: Temperature drift of oscillator mode is 3 times that of one-shot mode due to the addition of a second voltage comparator. Frequency always increases with an increasing temperature. Therefore it is possible to partially offset this drift with an offsetting temperature coefficient in the external resistor/capacitor combination.
4. Oscillator exhibits spurious oscillations on crossover points. Why?
   Answer: The 555 can oscillate due to feedback from power supply. Always bypass with sufficient capacitance close to the device for all applications.
5. Trying to drive a relay but 555 hangs up. How come?
   Answer: Inductive feedback. A clamp diode across the coil prevents the coil from driving Pin 3 below a negative 0.6V. This negative voltage is sufficient in some cases to cause the timer to malfunction. The solution is to drive the relay through a diode, thus preventing Pin 3 from ever seeing a negative voltage.
6. Double triggering of the TTL loads sometimes occurs. Why?
   Answer: Due to the high current capability and fast rise and fall times of the output, a totem-pole structure different from the TTL classical structure was used. Near TTL threshold this output exhibits a crossover distortion which may double trigger logic. A 1000pF capacitor from the output to ground will eliminate any false triggering.
7. What is the longest time I can get out of the timer?
   Answer: Times exceeding an hour are possible, but not always practical. Large capacitors with low leakage specs are quite expensive. It becomes cheaper to use a countdown scheme (see Figure 15) at some point, dependent on required accuracy. Normally 20 to 30 min. is the longest feasible time.

DESIGN FORMULAS

Before entering the section on specific applications it is advantageous to review the timing formulas. The formulas given here apply to the 555 and 556 devices.

APPLICATIONS

The timer, since introduction, has spurred the imagination of thousands. Thus, the ways in which this device has been used are far too numerous to present each one. A review of the basic operation and basic modes has previously been given. Presented here are some ingenious applications devised by our applications engineers and by some of our customers.

Missing Pulse Detector

Using the circuit of Figure 10a, the timing cycle is continuously reset by the input pulse train. A change in frequency, or a missing pulse, allows completion of the timing cycle which causes a change in the output level. For this application, the time delay should be set to be slightly longer than the normal time between pulses. Figure 10b shows the actual waveforms seen in this mode of operation.

Figure 11b shows the waveforms of the timer in Figure 11a when used as a divide-by-three circuit. This application makes use of the fact that this circuit cannot be retriggered during the timing cycle.

Pulse Width Modulation (PWM)

In this application, the timer is connected in the monostable mode as shown in Figure 12a. The circuit is triggered with a continuous pulse train and the threshold voltage is modulated by the signal applied to the control voltage terminal (Pin 5). This has the effect of modulating the pulse width as the control voltage varies. Figure 12b shows the actual waveform generated with this circuit.

Pulse Position Modulation (PPM)

This application uses the timer connected for astable (free-running) operation, Figure 13a, with a modulating signal again applied to the control voltage terminal. Now the pulse position varies with the modulating signal, since the threshold voltage, and hence the time delay, is varied. Figure 13b shows the waveform generated for triangle-wave modulation signal.

Tone Burst Generator

The 556 Dual Timer makes an excellent tone burst generator. The first half is connected as a one-shot and the second half as an oscillator (Figure 14).

The pulse established by the one-shot turns on the oscillator, allowing a burst to be generated.

Sequential Timing

One feature of the dual timer is that by utilizing both halves it is possible to obtain sequential timing. By connecting the output of the first half to the input of the second half via a 0.001µF coupling capacitor, sequential timing may be obtained. Delay t_1 is determined by the first half and t_2 by the second half delay (Figure 15).

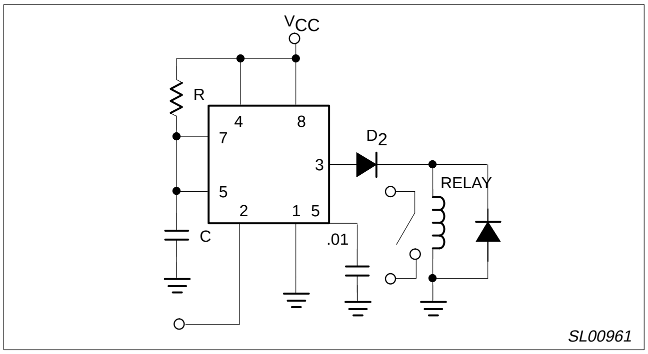


Figure 8. Driving High Q Inductive Loads

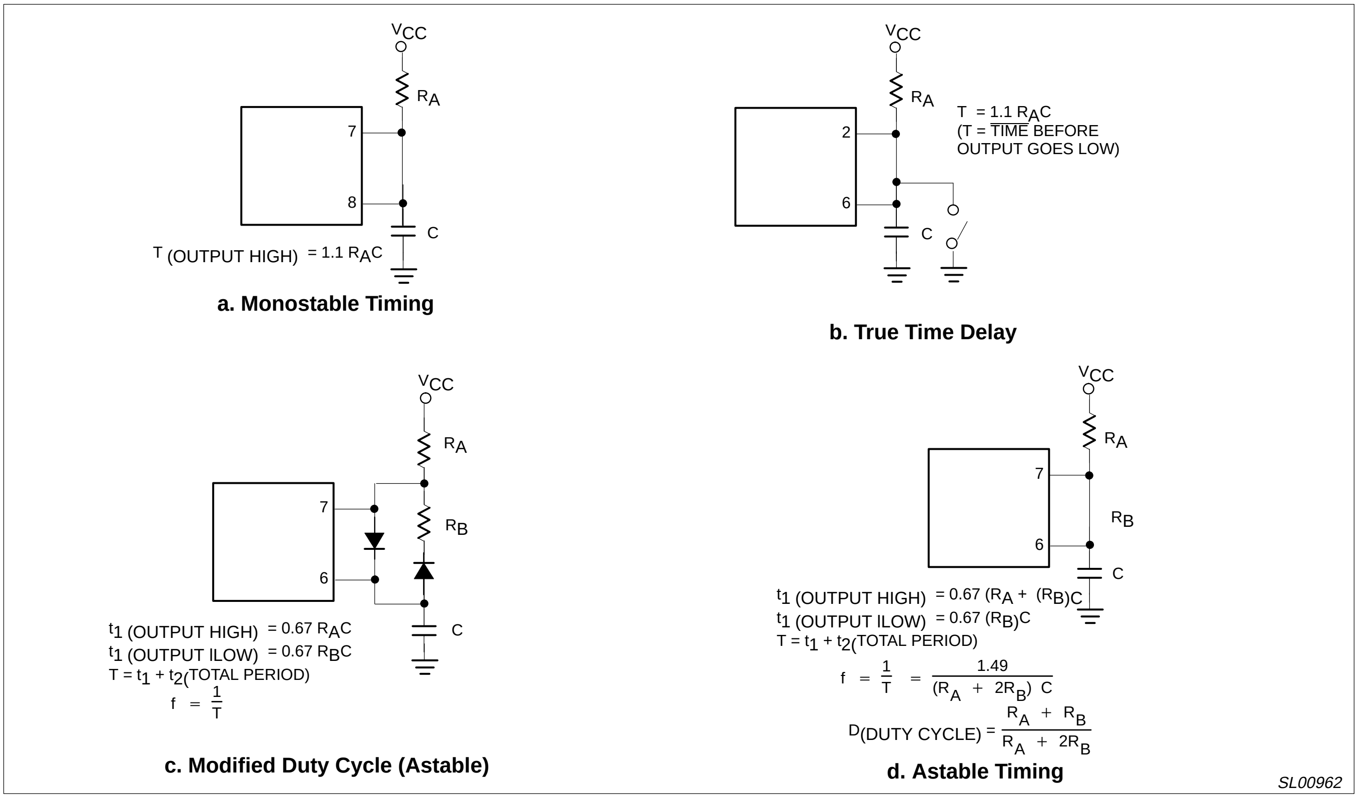


Figure 9.

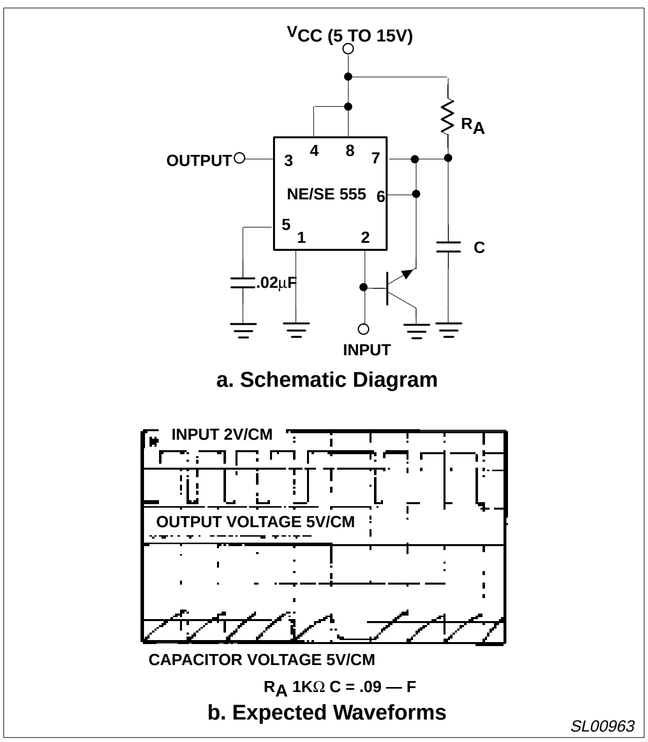


Figure 10.

The first half of the timer is started by momentarily connecting Pin 6 to ground. When it is timed-out (determined by 1.1 R_1C_1) the second half begins. Its duration is determined by 1.1 R_2C_2.

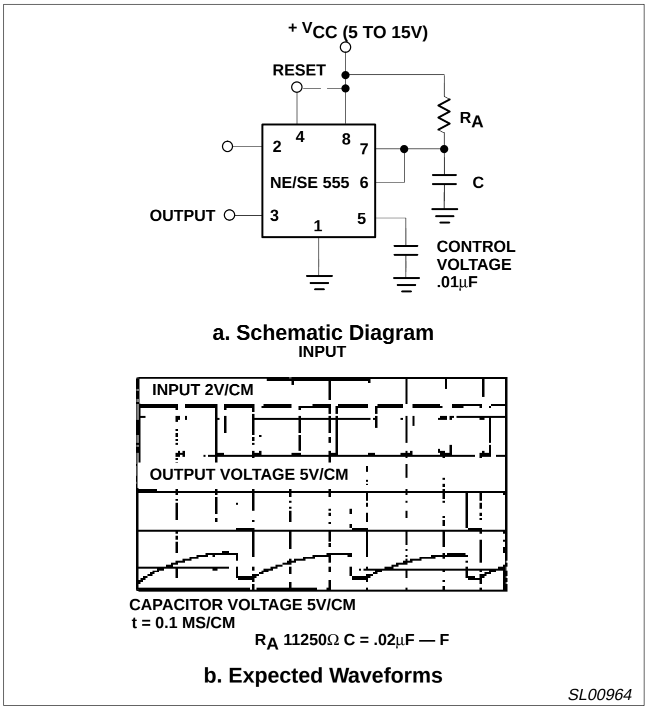


Figure 11.

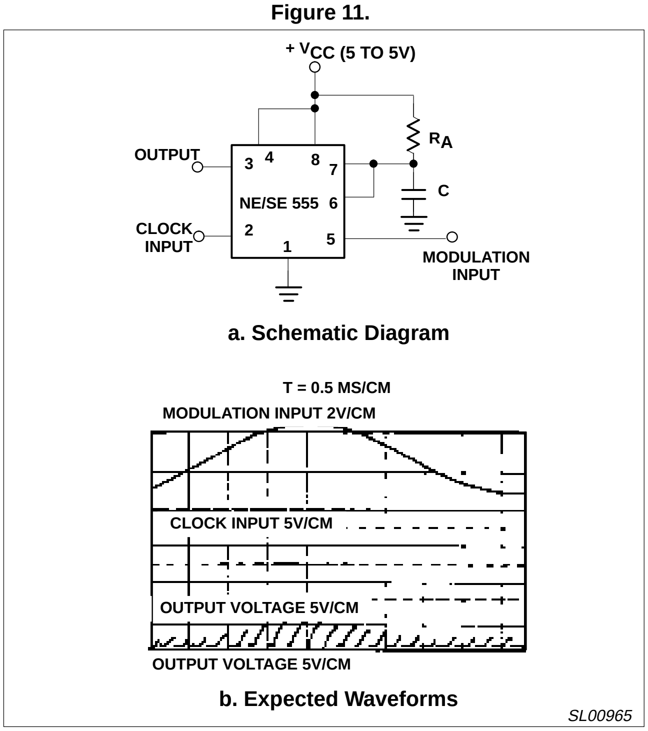


Figure 12.

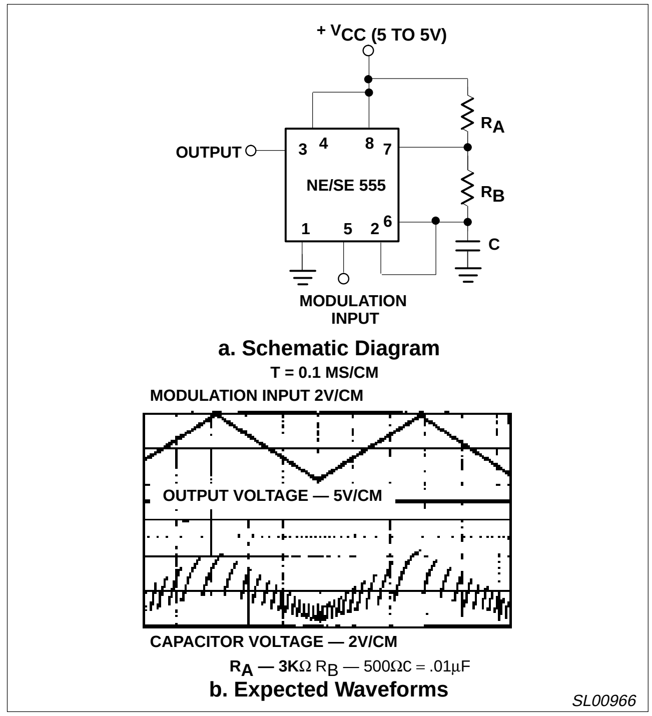


Figure 13.

Long Time Delays

In the 556 timer the timing is a function of the charging rate of the external capacitor. For long time delays, expensive capacitors with extremely low leakage are required. The practicality of the components involved limits

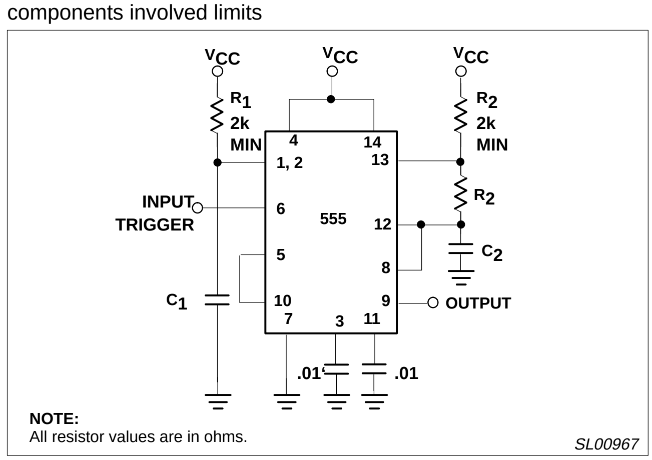


Figure 14. Tone Burst Generator

the time between pulses to around twenty minutes.

To achieve longer time periods, both halves may be connected in tandem with a “divide-by” network in between.

The first timer section operates in an oscillatory mode with a period of $1/f_O$. This signal is then applied to a "divide-by-N" network to give an output with the period of N/f_O. This can then be used to trigger the second half of the 556. The total time is now a function of N and f_O (Figure 16).

Speed Warning Device

Utilizing the "missing pulse detector" concept, a speed warning device, such as depicted, becomes a simple and inexpensive circuit (Figure 17a).

Car Tachometer

The timer receives pulses from the distributor points. Meter M receives a calibrated current thru R_6 when the timer output is high. After time-out, the meter receives no current for that part of the duty cycle. Integration of the variable duty cycle by the meter movement provides a visible indication of engine speed (Figure 18).

Oscilloscope-Triggered Sweep

The 555 timer holds down the cost of adding a triggered sweep to an economy oscilloscope. The circuit's input op amp triggers the timer, setting its flip-flop and cutting off its discharge transistor so that capacitor C can charge. When capacitor voltage reaches the timer's control voltage ($0.33V_{CC}$), the flip-flop resets and the transistor conducts, discharging the capacitor (Figure 19).

Greater linearity can be achieved by substituting a constant-current source for the frequency adjust resistor (R).

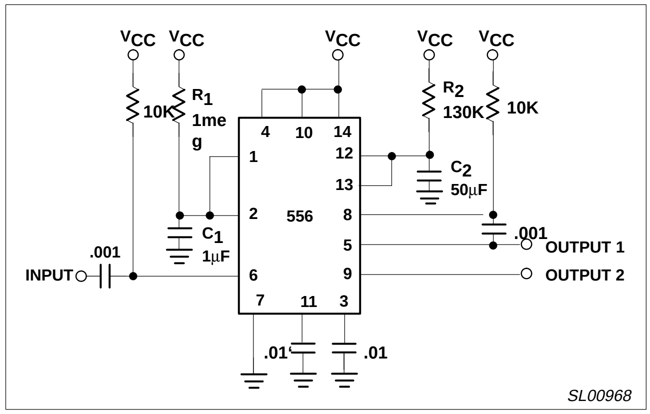


Figure 15. Sequential Timer

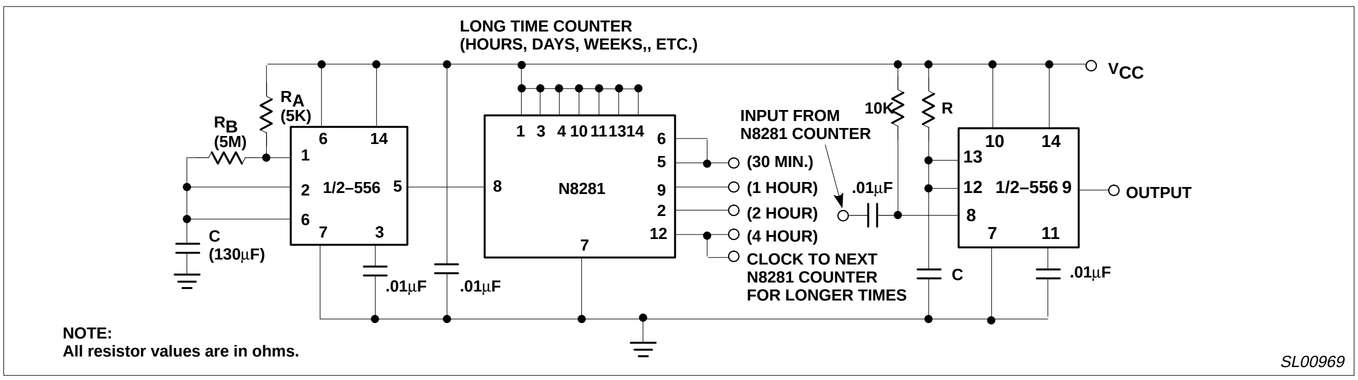
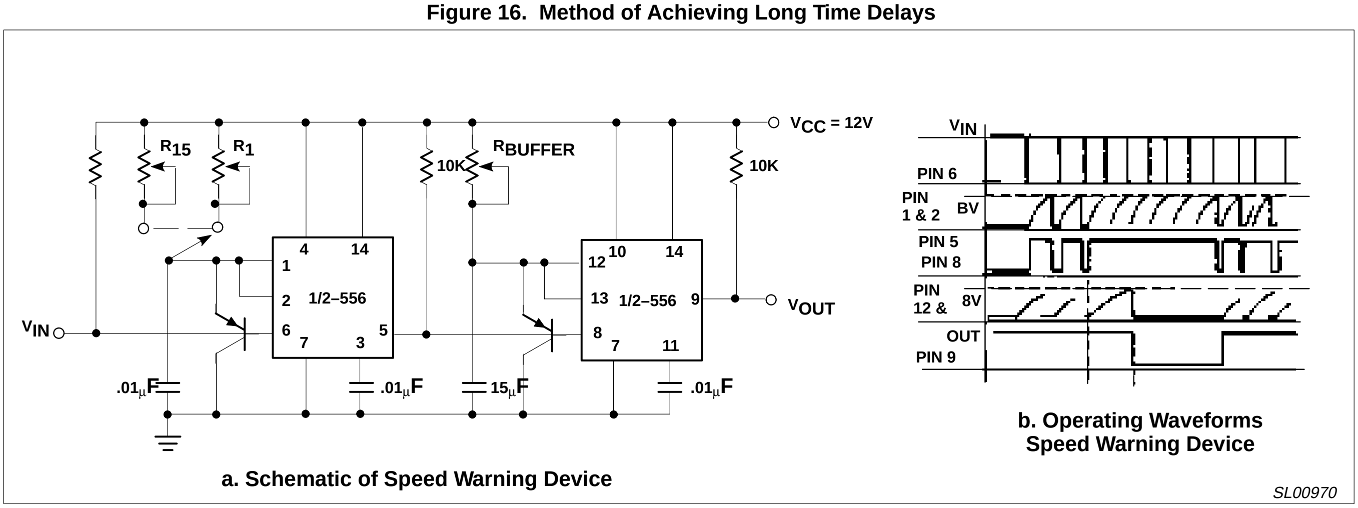


Figure 16. Method of Achieving Long Time Delays



a. Schematic of Speed Warning Device

b. Operating Waveforms Speed Warning Device

Figure 17.

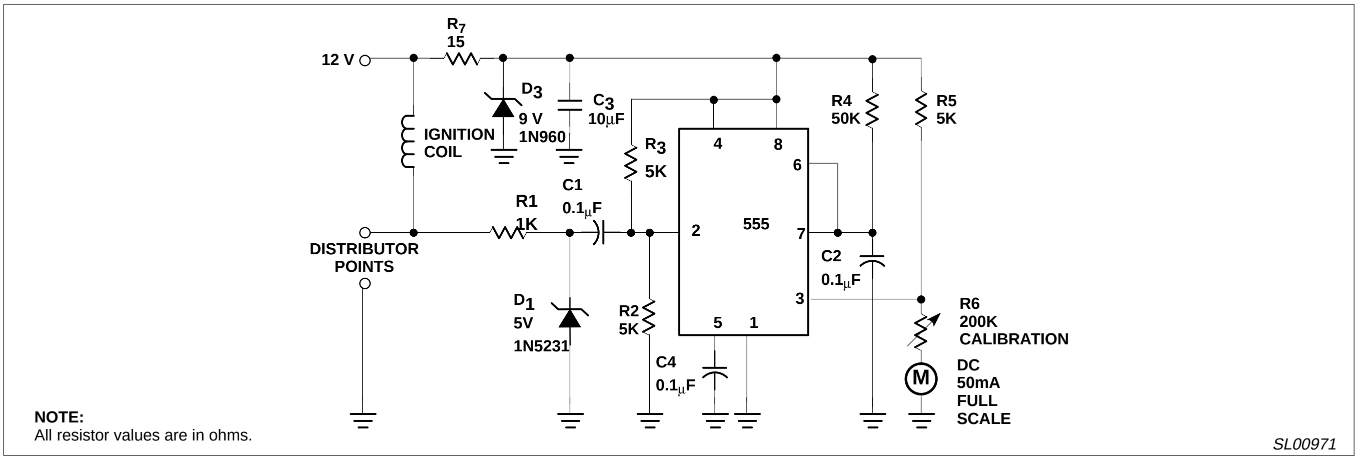


Figure 18. Tachometer

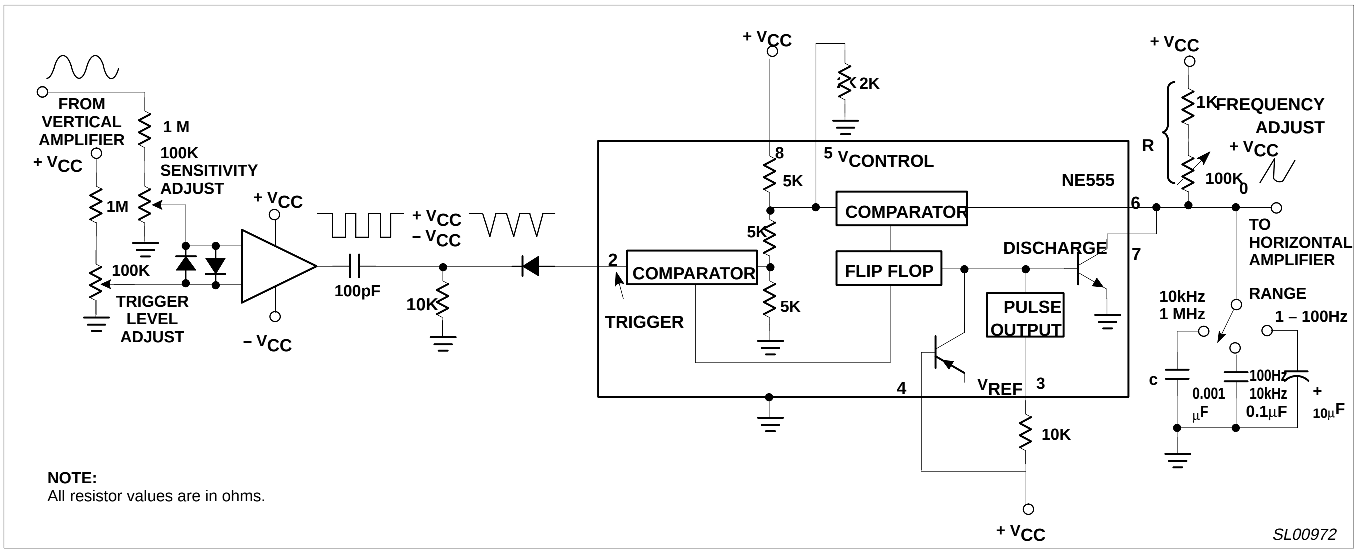


Figure 19. Schematic of Triggered Sweep

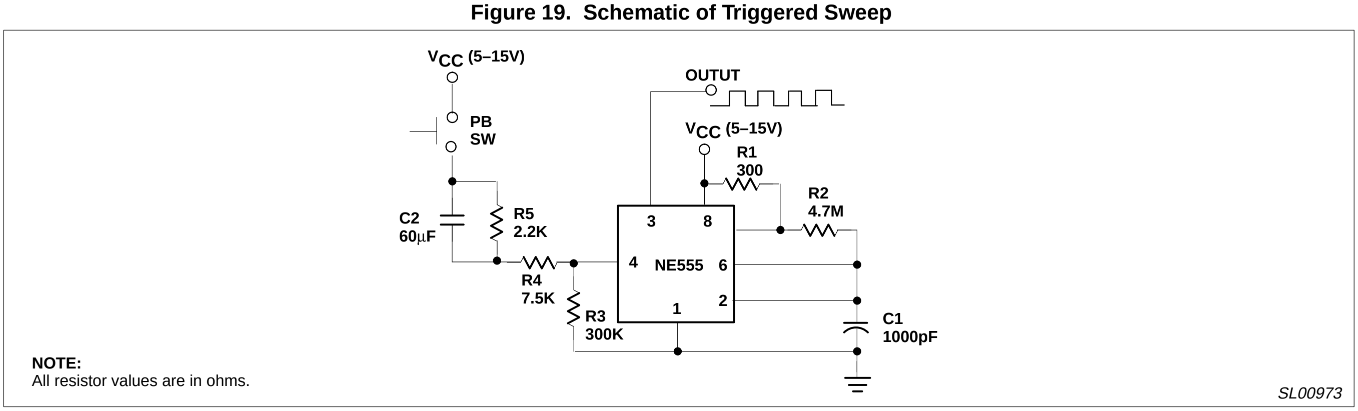


Figure 20. Square Wave Tone Burst Generator

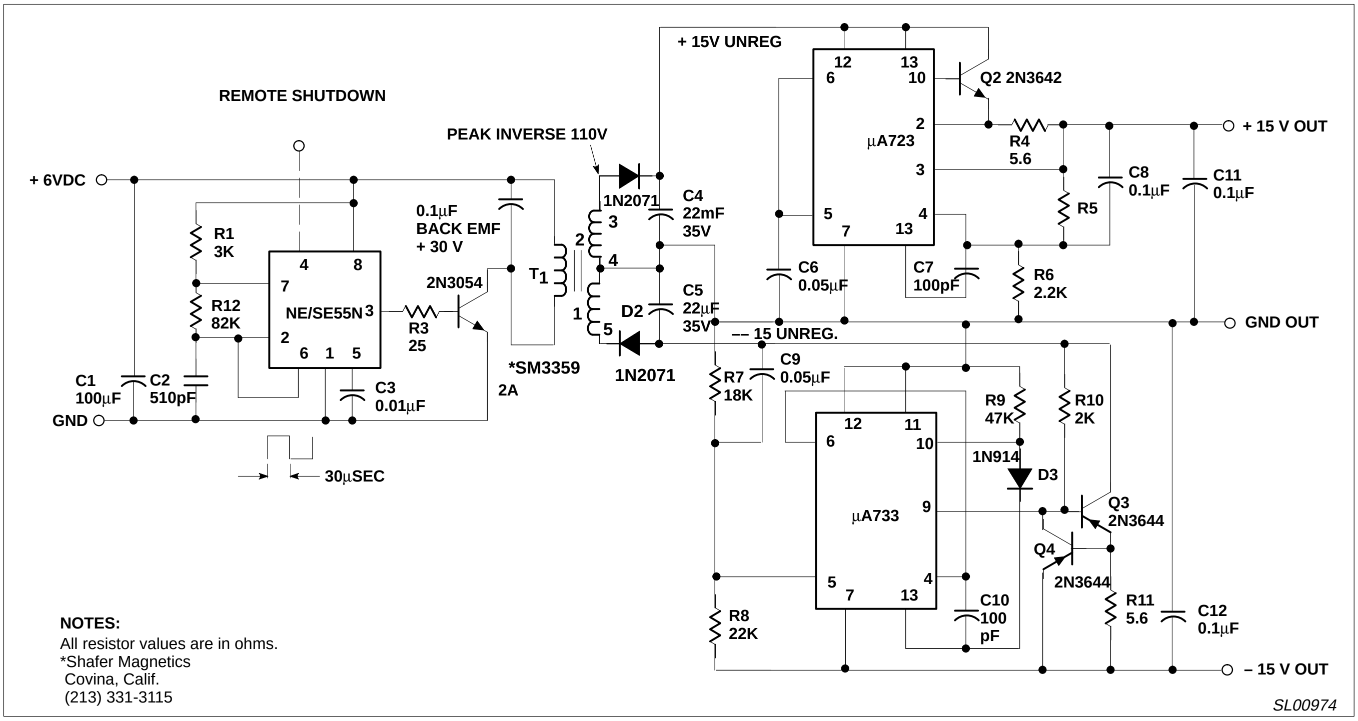


Figure 21. Regulated DC-to-DC Converter

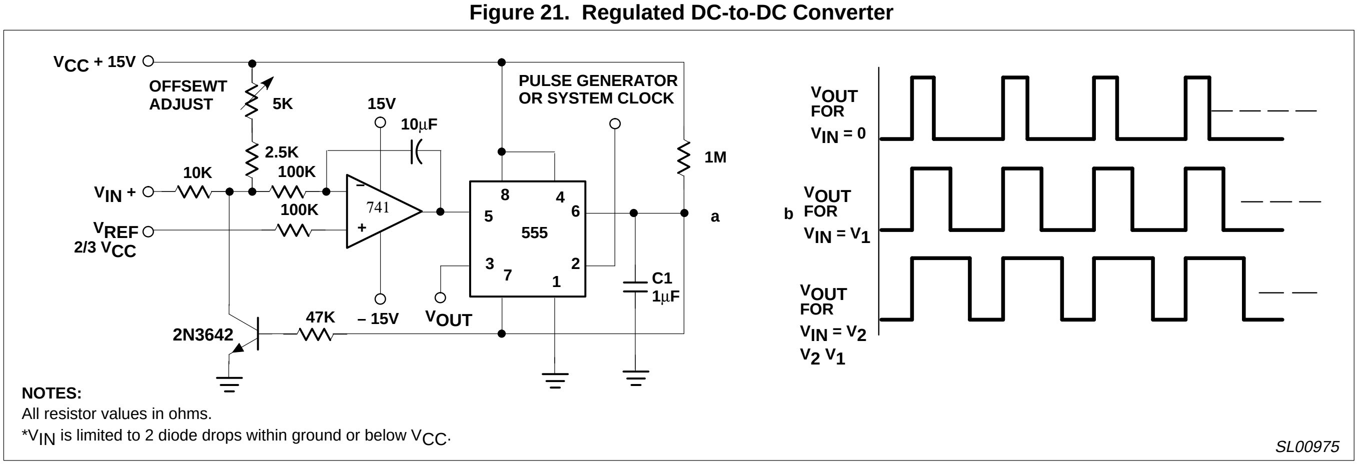


Figure 22. Voltage-to-Pulse Duration Converter

Square Wave Tone Burst Generator

Depressing the pushbutton provides square wave tone bursts whose duration depends on the duration for which the voltage at Pin 4 exceeds a threshold. Components R_1, R_2 and C_1 cause the astable action of the timer IC (Figure 20).

Regulated DC-to-DC Converter

Regulated DC-to-DC converter produces $15V_{DC}$ outputs from a $+5V_{DC}$ input. Line and load regulation is 0.1% (Figure 21).

Voltage-to-Pulse Duration Converter

Voltage levels can be converted to pulse durations by combining an op amp and a timer IC. Accuracies to better than 1% can be obtained with this circuit (a), and the output signals (b) still retain the original frequency, independent of the input voltage (Figure 22).

Servo System Controller

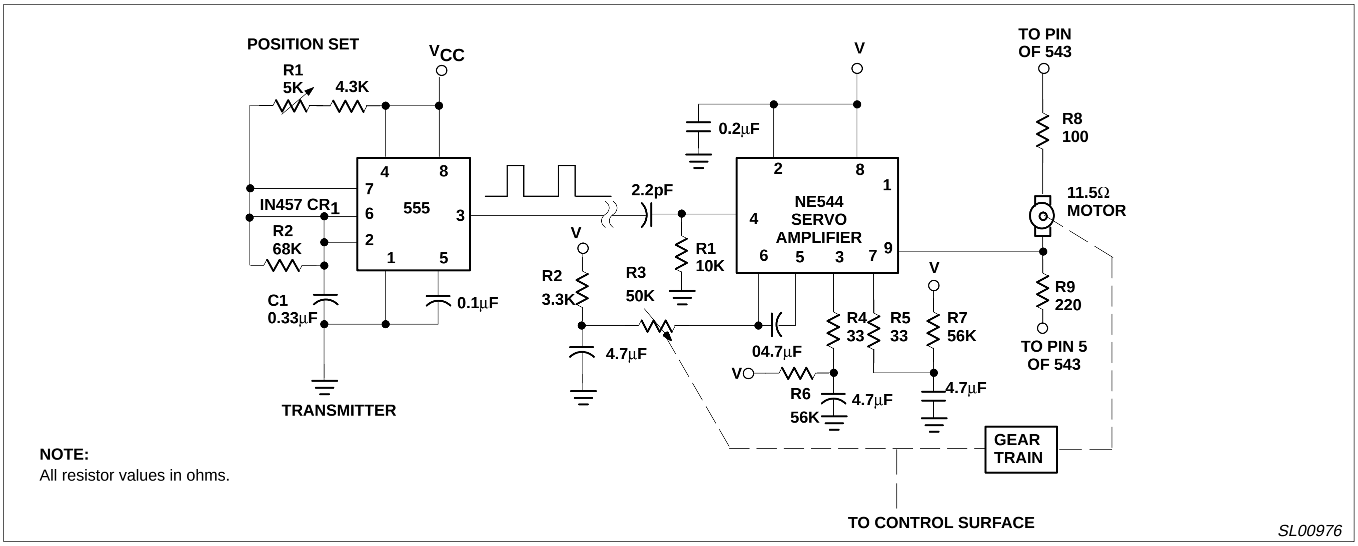
To control a servo motor remotely, the 555 needs only six extra components (Figure 23).

Stimulus Isolator

Stimulus isolator uses a photo-SCR and a toroid for shaping pulses of up to 200V at 200μA (Figure 24).

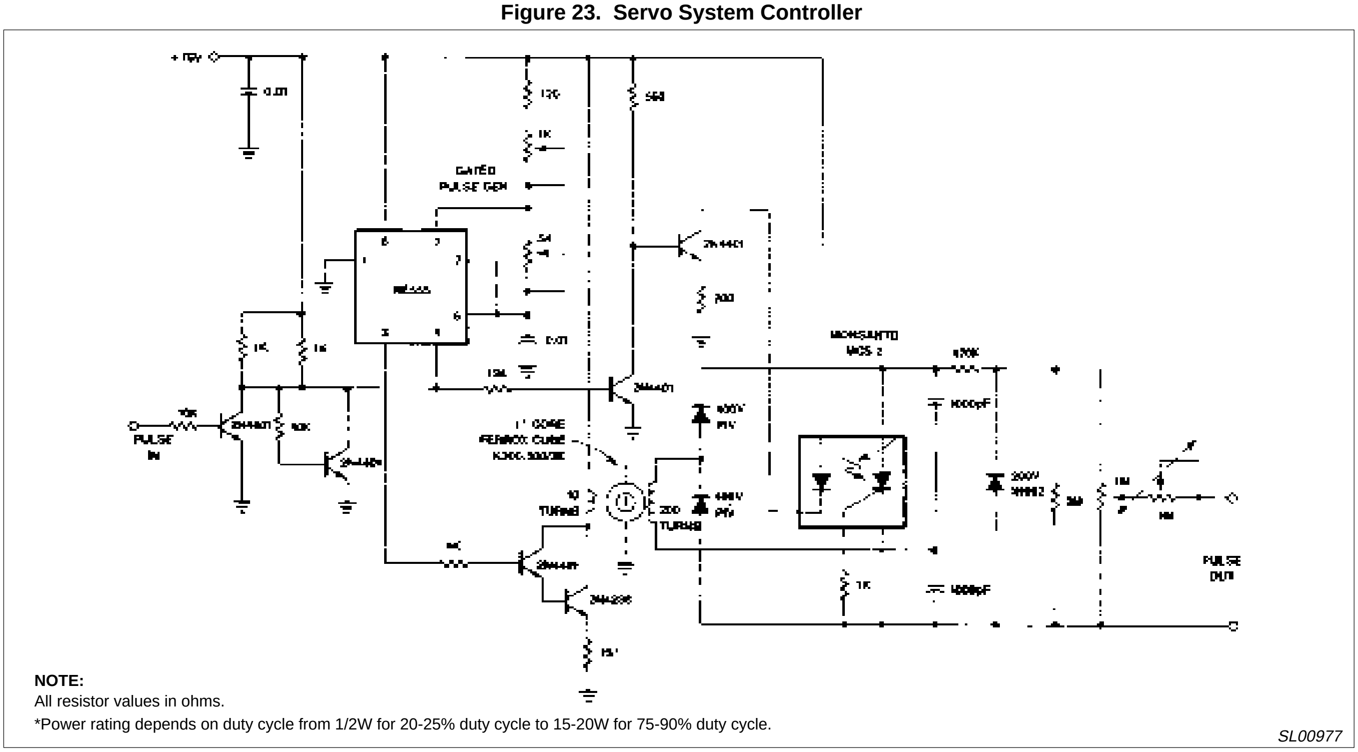
Voltage-to-Frequency Converter (0.2% Accuracy)

Linear voltage-to-frequency converter (a) achieves good linearity over the 0 to -10V range. Its mirror image (b) provides the same linearity over the 0 to +10V range, but is not DTL/TTL compatible (Figure 25).



NOTE:
All resistor values in ohms.

Figure 23. Servo System Controller



NOTE:
All resistor values in ohms.
*Power rating depends on duty cycle from 1/2W for 20-25% duty cycle to 15-20W for 75-90% duty cycle.

Figure 24. Stimulus Isolator

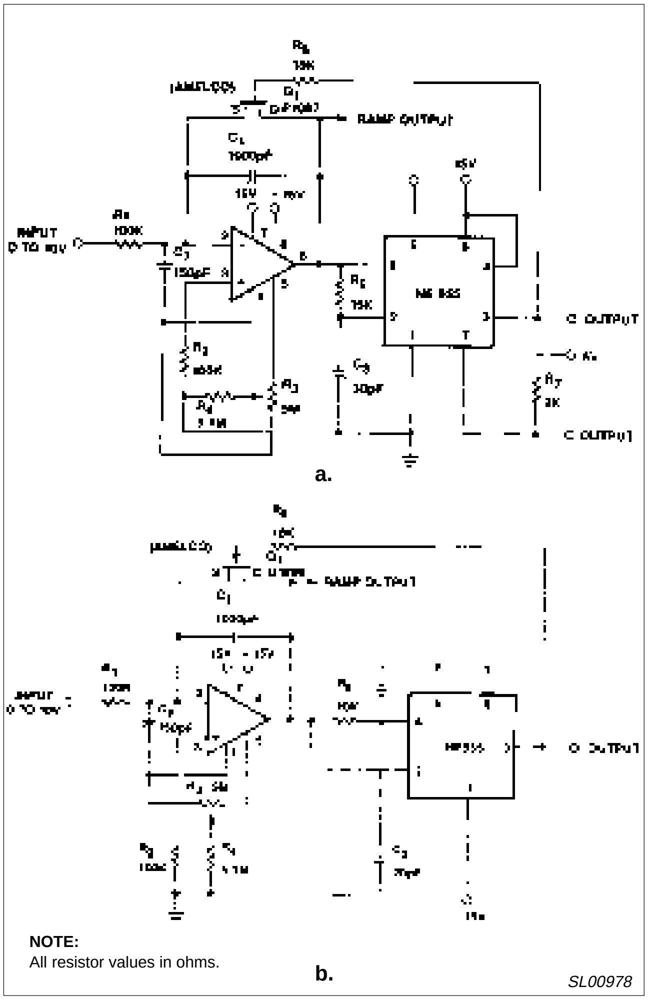


Figure 25.

Positive-to-Negative Converter

Transformerless DC-DC converter derives a negative supply voltage from a positive. As a bonus, the circuit also generates a clock signal.

The negative output voltage tracks the DC input voltage linearity (a), but its magnitude is about 3V lower. Application of a 500Ω load, (b), causes 10% change from the no-load value (Figure 26).

Auto Burglar Alarm

Timer A produces a safeguard delay, allowing driver to disarm alarm and eliminating a vulnerable outside control switch. The SCR prevents timer A from triggering timer B, unless timer B is triggered by strategically-located sensor switches (Figure 27).

Cable Tester

Compact tester checks cables for open-circuit or short-circuit conditions. A differential transistor pair at one end of each cable line remains balanced as long as the same clock pulse-generated by the timer IC appears at both ends of the line. A clock pulse just at the clock end of the line lights a green light-emitting diode, and a clock pulse only at the other end lights a red LED (Figure 28).

Low Cost Line Receiver

The timer makes an excellent line receiver for control applications involving relatively slow electromechanical devices. It can work without special drivers over single unshielded lines (Figure 29).

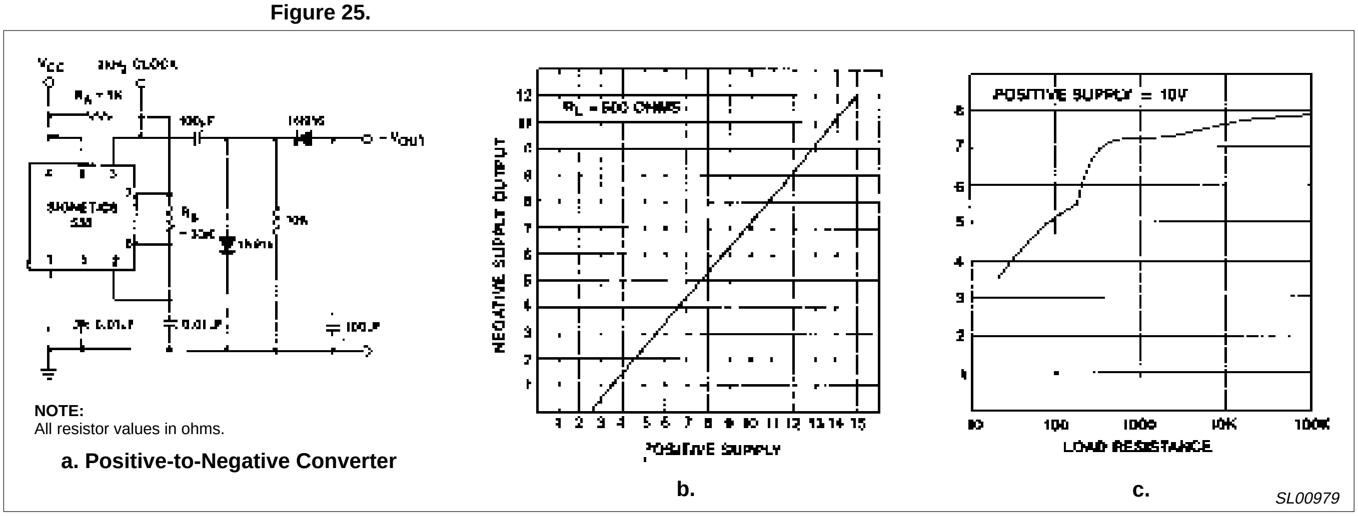
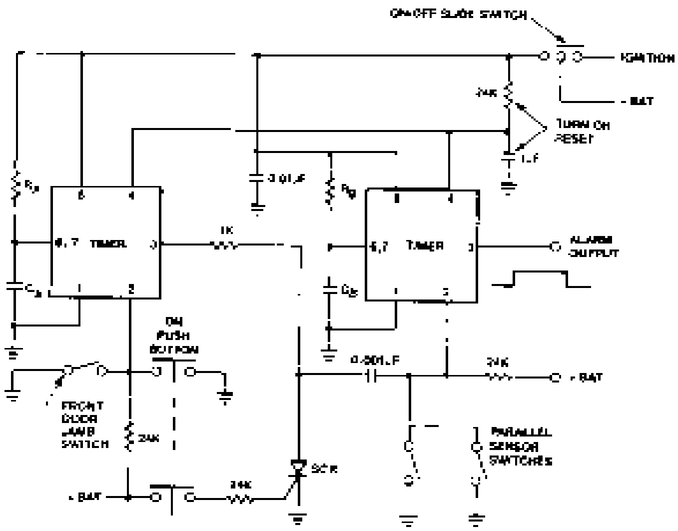


Figure 26.



NOTES:
Timer Philips Semiconductors NE555
All resistor values in ohms.

SL00980

Figure 27. Auto Burglar Alarm

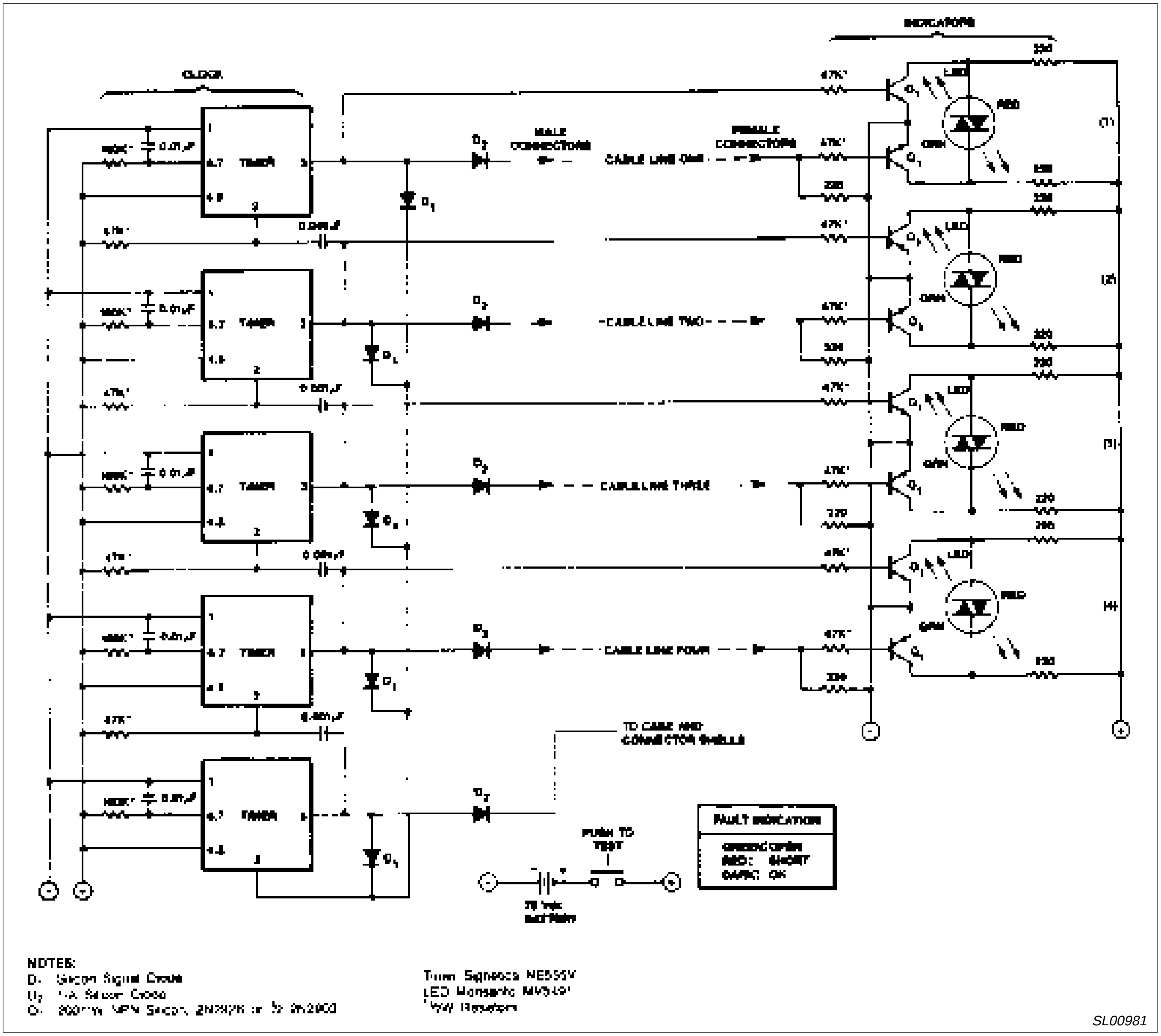


Figure 28. Cable Tester

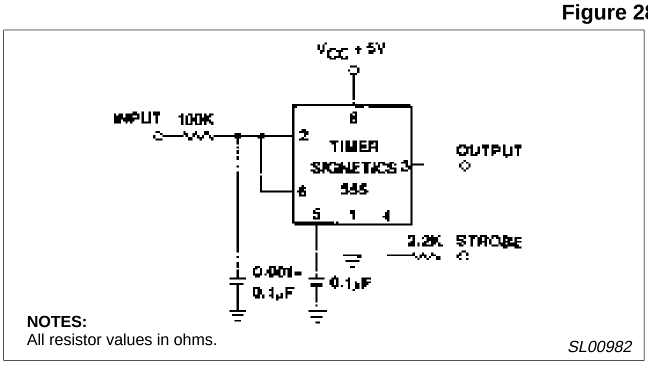


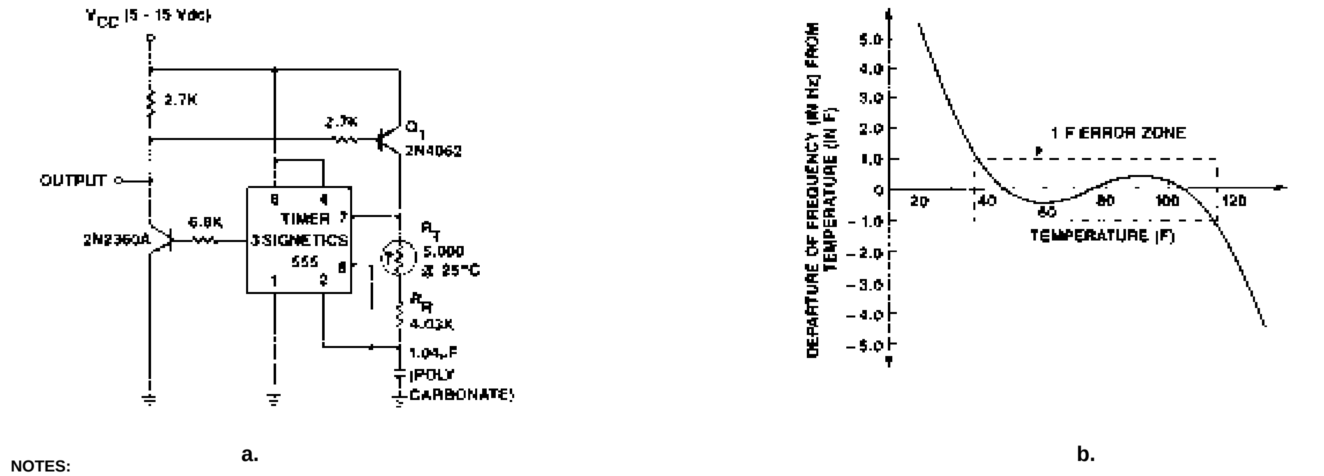
Figure 29. Low Cost Line Receiver

Temperature Control

A couple of transistors and thermistor in the charging network of the 555-type timer enable this device to sense temperature and produce a corresponding frequency output. The circuit is accurate to within ±1Hz over a 78°F temperature range (Figure 30).

Automobile Voltage Regulator

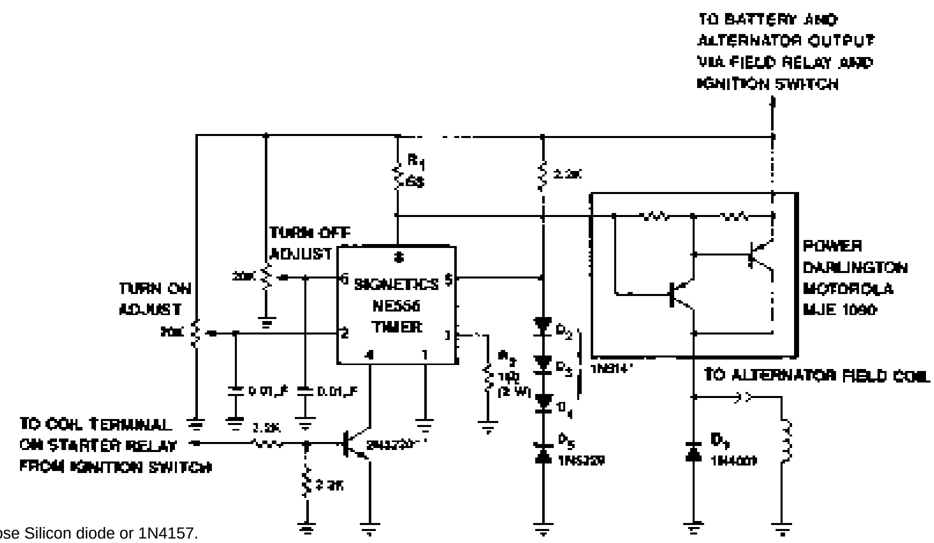
A monolithic 555-type timer is the heart of this simple automobile voltage regulator. When the timer is off so that its output (Pin 3) is low, the power Darlington transistor pair is off. If battery voltage becomes too low (less than 14.4V in this case), the timer turns on and the Darlington pair conducts (Figure 31).



NOTES:
All resistor values in ohms.

SL00983

Figure 30. Temperature Control

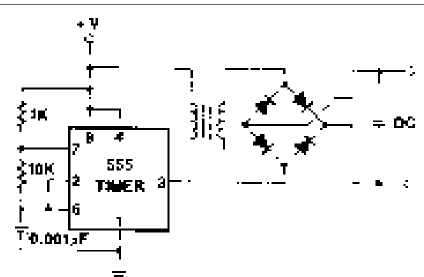


NOTES:
* Can be any general purpose Silicon diode or 1N4157.
** Can be any general purpose Silicon transistor.
All resistor values are in ohms.

SL00984

Figure 31. Automobile Voltage Regulator

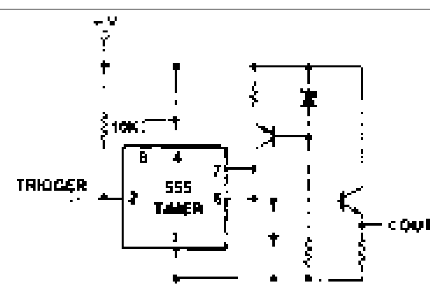
DC-to-DC Converter



SL00985

Figure 32. DC-to-DC Converter

Ramp Generator



SL00986

Figure 33. Ramp Generator

Ramp Generator

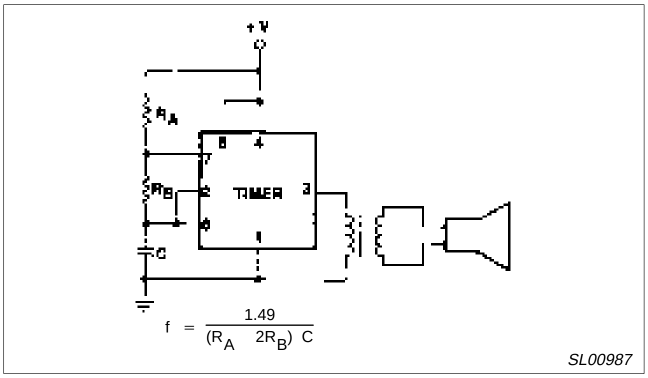


Figure 34. Ramp Generator

Low Power Monostable Operation

In battery-operated equipment where load current is a significant factor, Figure 35 can deliver 555 monostable operation at low standby power. This circuit interfaces directly with CMOS 4000 series and 74L00 series. During the monostable time, the current drawn is 4.5mA for T=1.1RC. The rest of the time the current drawn is less than 50µA. (Circuit submitted by Karl Imhof, Executone Inc., Long Island City, NY.)

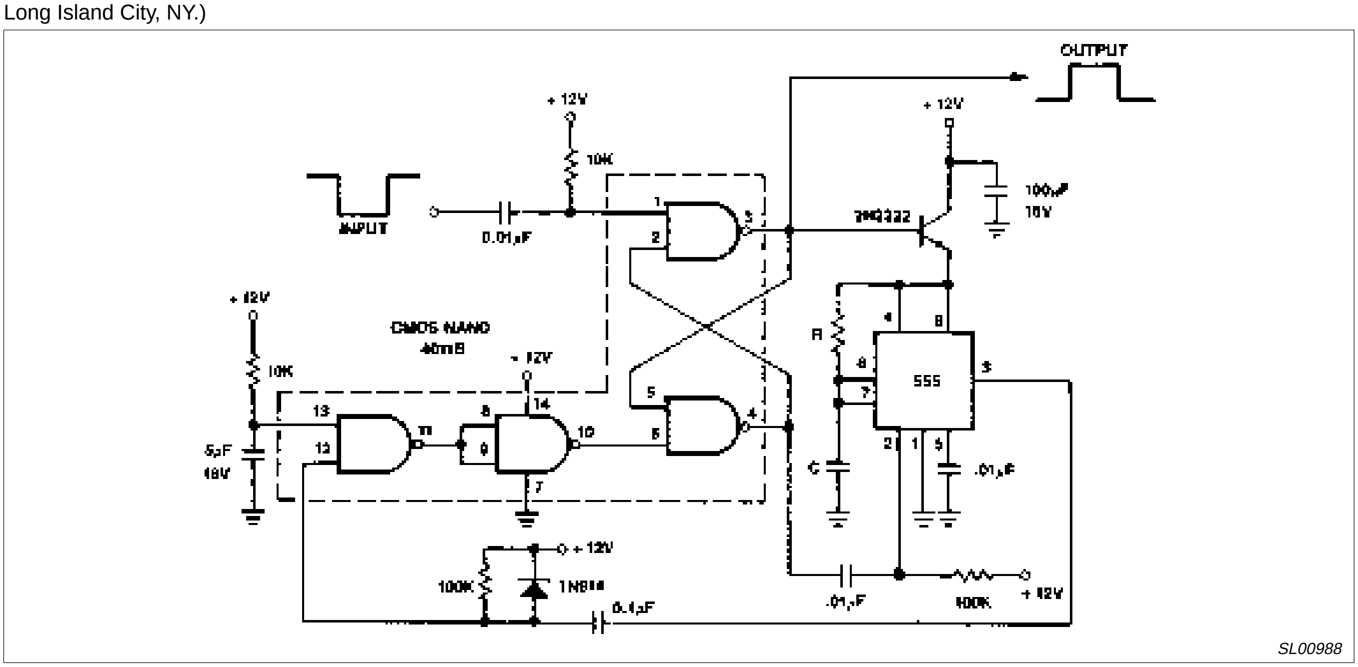


Figure 35. Low Power Monostable

Theory of Operation

The missing pulse detector (see Figure 10) operates as a triggered monostable multivibrator but with the added feature that the output signal remains high for a repetitive pulse condition at the trigger input node. This is accomplished by the addition of a reset inhibit function which prevents the normal time-out of the timer as long as there are input pulses present with period less than the time delay period. The circuit which provides this feature is an external PNP transistor with its base tied in parallel with the trigger input pin.

As the input pulse waveform exceeds the instantaneous timing coapacitor voltage by one V_{BE} in the negative direction, the PNP transistor is turned on momentarily, pulling the capacitor voltage toward ground potential. This incremental discharge action prevents the threshold voltage on Pin 6 from activating the reset action of the timer if the time delay between input pulses is shorter than the programmed time delay set by the external R/C network. This inhibit action occurs whenever the timing capacitor is prevented from exceeding 2/3 V_{CC}. Note that the degree of capacitor discharge is directly proportional to the duration of the turn-on time of the external PNP transistor. The capacitor voltage is equal to charge Q/capacitance C. The amount of delta V_C per input pulse is (I_C x T_P (sec)) / C(F) where T_P is the width of the trigger pulse and IC is the collector current of the PNP transistor during the duration of the trigger pulse. The inhibit condition is fulfilled by making the time constant of the RC network, connected to Pin 6 and 7, somewhat longer than the interpulse period for normal fault free operation. The

In other low power operations of the timer where V_{CC} is removed until timing is needed, it is necessary to consider the output load. If the output is driving the base of a PNP transistor, for example, and its power is not removed, it will sink current into Pin 3 to ground and use excessive power. Therefore, when driving these types of loads, one should recall this internal sinking path of the timer.

output will then remain positive until such a fault is long than the RC time constant. The missing pulse detector then provides a negative going output pulse proportional to the number of missing pulses received at the input.

The Speed Warning Circuit

Figure 17 shows an application which uses two missing pulse detectors in tandem as an aover-speed sensor. A speed transducer pulse signal of negative polarity is fed into the first stage of the NE556 which is actually used in the mode for which the timer is always allowed to time out if the pulse rate is below the desired speed threshold. This occurs, as discussed above, if the pulse input period is longer than the natural time-out period of the timer (as determined by the external RC network). The wavetrain coming from the first stage continually toggles for a speed condition below the set point. Next, stage one output signal is fed directly into the trigger input, Pin 8, of the second stage of the NE556, and simultaneously to the base of the external PNP discharge transistor. The second stage operation is identical to the one described in the missing pulse detector section above. The second stage timer output is held high when the speed transducer pulse train rate is below the critical threshold. This stage of the dual timer acts to alter the dynamic response of the speed detector so that a number of pulses must be missed to activate its output. This gives the detector a form of hysteresis and prevents the occurance of intermittent output signaling due to an instantaneous over speed condition. The length of the stage-two time delay threshold is programmed by adjusting R_{BUFFER}.

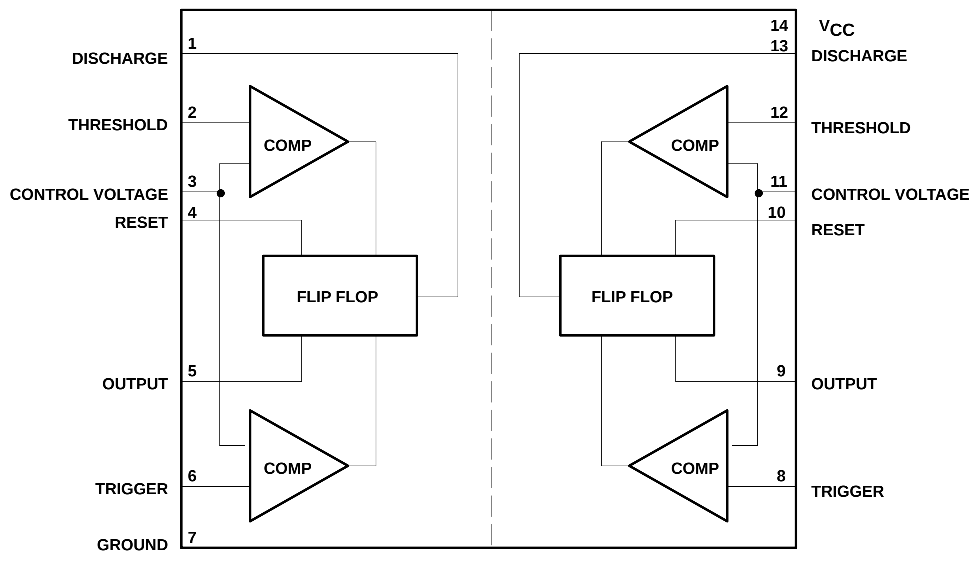


Figure 36. Block Diagram

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